VGA CMOS Digital Image Sensor

General Descriptions

BG0316 is a high performance VGA CMOS image sensor with on-chip Intelligent Power Management Unit. BG0316 provides superior quality image by integrating a high performance analog signal processor, which includes wide range programmable gain amplifiers and a 10-bits A/D converter. The pixel's offset and black level is automatically compensated by an on-chip full feedback-loop circuit. Furthermore, BG0316 provides maximum user flexibility by programming on-chip control registers through a 2-wire serial control interface. It can be configured to operate based on various parameters such as exposure time, frame rate, active window location/size/decimation, row and column mirroring, and different power schemes. BG0316 also incorporates an experiment mode of 32 line global exposure mode.

Features

- 2-wire serial control interface.
- Internal Power On Reset.
- Internal regulator of VDD core.
- Package options include CSP.
- Bare Die

Applications

- High speed gaming system

Key Specifications

Lens format	1/7inch
Active pixel array	645 x 485
Pixel size	3.20um x 3.20um
Active pixel array Area	2064um x 1552 um
Frame rate	VGA 120fps
Color filter array	RGB Bayer
Shutter Type	Electronic Rolling/Global shutter
SNR	40dB@22℃
Dynamic range	65dB@22℃
Max Clock Freq	50M
Max Analog Gain	16X
Power supply	Digital internal 1.5v IO 2.7v ~3.3v Analog 2.7v ~3.3v
Power Consumption	170mW@120fps
Standby Current	<1mA
Operating temperature	-25 – 60 ℃
Package	COB
Bare Die	
CRA	25

1 IO Descriptions & Typical Configuration

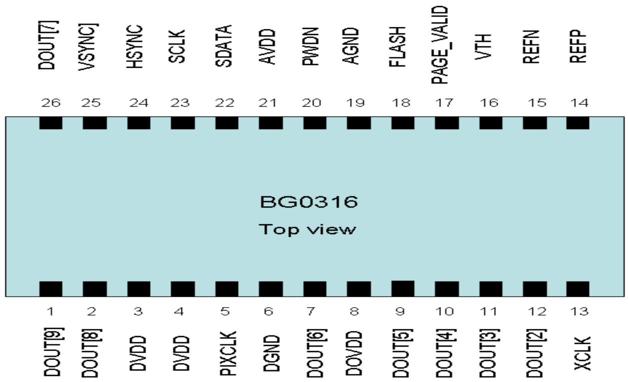

Figure 1 PAD diagram

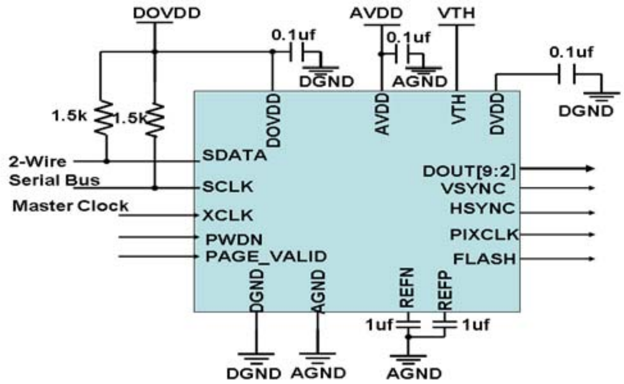

Figure 2 Typical Configuration

PAD No.	Name	Type	Description
1	DOUT[9]	Out	Pixel Data Output Bit9.
2	DOUT[8]	Out	Pixel Data Output Bit8.
3	DVDD	Power	Digital core Power.
4	DVDD	Power	Digital core Power.
5	PIXCLK	Out	Pixel Clock Output. Pixel data outputs are valid during rising edge of this clock.
6	DGND	Power	Digital ground.
7	DOUT[6]	Out	Pixel Data Output Bit 6.
8	DOVDD	Power	I/O Power.
9	DOUT[5]	Out	Pixel Data Output Bit 5.
10	DOUT[4]	Out	Pixel Data Output Bit4.
11	DOUT[3]	Out	Pixel Data Output Bit3.
12	DOUT[2]	Out	Pixel Data Output Bit2.
13	XCLK	In	Master Clock into sensor
14	REFP	In/Out	Voltage Reference P.
15	REFN	In/Out	Voltage Reference N.
16	VTH	Power	Charge pump voltage.
17	PAGE_VALID	In/Out	Input mode: Page trigger. Output mode: Pixel Data Output Bit1.
18	FLASH	Out	Shutter time flag in global shutter mode. When high, sensor pixel in shutter.
19	AGND	Power	Analog ground.
20	PWDN	In/Out	Input mode: Standby mode control. When high, chip enters standby mode. All operations are stopped. Output mode: Pixel Data Output Bit0.
21	AVDD	Power	Analog Power.
22	SDATA	In/Out	Serial bus data.
23	SCLK	In	Serial bus Clock.

24	HSYNC	Out	Active HIGH during line of selectable valid pixel data.
25	VSYNC	Out	Active HIGH during line of selectable valid pixel data.
26	DOUT[7]	Out	Pixel Data Output Bit 7.

2 Function blocks Description

Figure3 shows the function blocks diagram of the BG0316. The BG0316 can be put in a low power sleep mode by assert PWDN. Output video is stream via 8-bit parallel DOUT port. The clock pixclk is used to latch data while the vsync and hsync signal indicates active video. BG0316 include an Image Sensor Array, a Serial Control Interface, a Timing Control Unit, a PLL, an Analog Signal Conditioner (ASC), an Analog to Digital Converter (ADC) and a Post Processing Unit. The BG0316 is wholly controlled through 2-wire serial control interface.

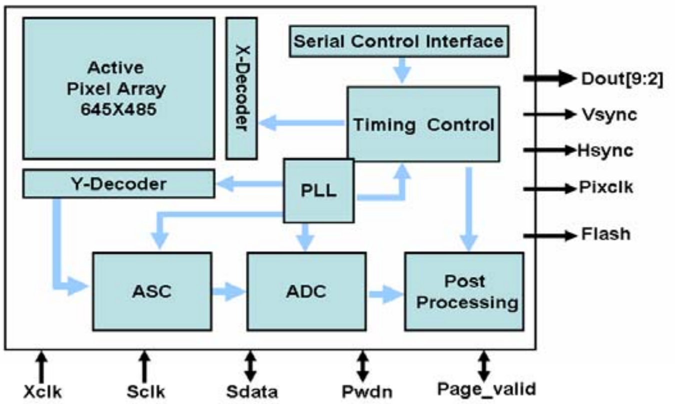

Figure 3 Functional Blocks Diagram

3 Image Sensor Array

The Image Senor Array contains a 645x485 active pixel array. The active pixel array is surrounded by dark rows and columns for automatic black level compensation. There are 12 dark rows on the top of the active pixel array, 6 dark columns on the right side of the active pixel array, 5 dark columns on the left side of the active pixel array, and 3 dark rows below the pixel array. The Image Sensor Array also contains the X-decoder (row decoder) and the Y-decoder (column decoder) not shown in Figure 3. BG0316 image sensor uses Bayer Pattern for its color filter design. The color filter mapping is shown in Figure 5.

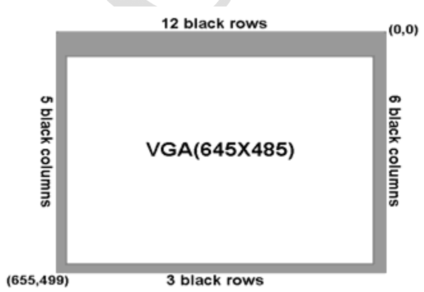

Figure 4 Active CMOS Pixel Array

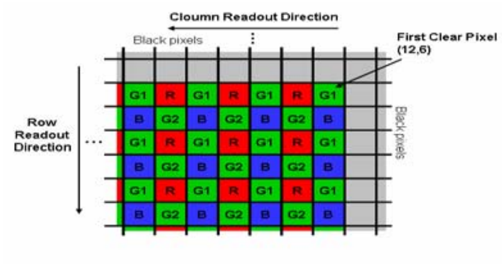

Figure 5 The pixel's color mapping

4 Serial Control Interface

The Serial Control Interface supports the data exchange between the sensor and its host through a simple 2 wire serial bus. The Serial Control Interface serves as a slave on the 2 wire serial bus while the host must serve as the master of the bus. The Serial Control Interface employs a simple 2 wire serial protocol defined and described in session 2.2.1 and 2.2.2. The 2 wire serial bus physically consists of two wires which connect to two pull up resistors external to the master and slave bus devices. The 2 wires are used to connect the clock and data lines of the master and slave devices. BG0316's serial clock input is named as SCLK of the serial bus and its serial data line IO pin is named as SDATA. And its slave address is 0x52, that is 0xa4 for writing mode and 0xa5 for reading mode.

The frequency of SCLK must be following the rule: $f_{sclk}<=f_{xclk}/16$.

4.1.1 A simple serial bus protocol and its implementation

The Serial Control Interface defines the following transmission codes:

- A start bit

  A start bit is implemented as a high-to-low transition of data line SDATA while the clock line SCLK is high
- A stop bit

  A stop bit is implemented as a low-to-high transition of data line SDATA while the clock line SCLK is high
- Master and slave devices sample SDATA on a low-to-high transaction of SCLK
- Master and slave devices apply new data on SDATA right after a high-to-low transaction of SCLK.
- 8-bit slave addressing byte

  The slave device address is the 7^{th} to 1^{st} bits of the 8-bit slave addressing byte. The LSB bit of the 8-bit slave addressing byte determines whether the transaction is a read or a write. It indicates a read when the LSB bit is '1'. It indicates a write when the LSB bit is '0'. This chip the slave address is 0xA4 for writing mode or 0xA5 for reading mode.
- An acknowledge bit or a no-acknowledge bit

  An acknowledge bit is implemented as a pull-down on the data line SDATA during the acknowledge clock cycle.

  A no-acknowledge bit is implemented as a no pull-down on the data line SDATA (SDATA remains a pull-up) during the acknowledge clock cycle
- 8-bit data

  The master and slave device send and receive data in 8 bit byte.

4.1.2 The read and write transactions

The Serial Control Interface supports four different read and write modes which are a single byte write mode, a single byte read mode, a burst write mode, and a burst read mode.

4.1.2.1 The Single Byte Write Mode

The single byte write mode sequence is defined as the following.

1. The master sends a start bit to the slave.
2. The master sends the slave device address with write mode.

3. The slave sends an acknowledge bit to the master to indicate receive its slave device address.
4. The master sends 8-bit register address to the slave.
5. The slave sends an acknowledge bit after it receives the 8-bit data.
6. The master sends 8-bit register data to the salve.
7. The slave sends an acknowledge bit after it receives the 8-bit data
8. The master sends a stop bit to the slave.

Figure 6 shows the single byte write mode, which write data 0x56 to register 0x2C.

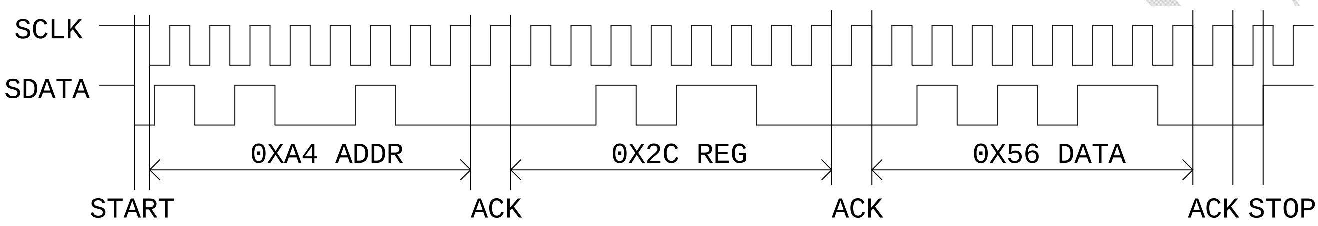

Figure 6 Single Byte Write Mode

4.1.2.2 Burst write mode

The burst write mode sequence is defined as the following.

1. The master sends a start bit to the slave.
2. The master sends the slave device address with write mode.
3. The slave sends an acknowledge bit to the master to indicate receive its slave device address.
4. The master sends 8-bit register address to the slave.
5. The slave sends an acknowledge bit after it receives the 8-bit data.
6. The master sends 8-bit register data to the slave.
7. The slave sends an acknowledge bit to master.
8. The master continues to send the next register data by repeating step6 and 7 and the slave increases the register address by one automatically.
9. The master stops writing by sending a stop bit.

Figure 7 shows the burst write sequence, which write data 0x56 to register 0x2C and 0x75 to register 0x2D.

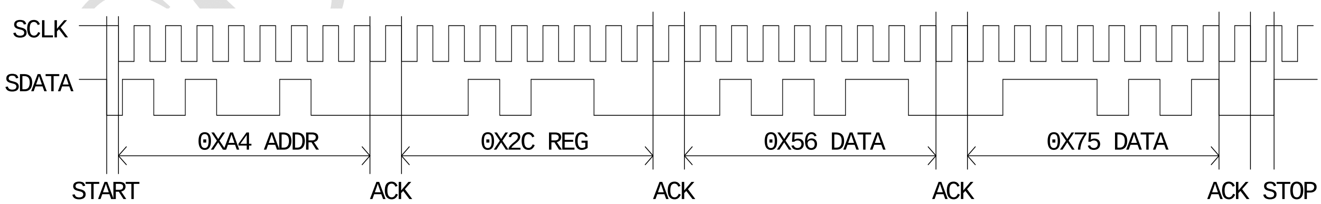

Figure 7 Burst Write Mode

4.1.2.3 Single byte read mode

The byte read mode sequence is defined as the following.

1. The master sends a start bit to the slave.
2. The master sends the slave device address with write mode.
3. The slave sends an acknowledge bit to the master.
4. The master sends 8-bit register address to the slave.
5. The slave sends an acknowledge bit to the master.
6. The master sends a start bit to the slave.
7. The master sends the slave device address with read mode.
8. The slave sends an acknowledge bit to the master.
9. The slave sends 8-bit data to the master
10. The master sends a no-acknowledge bit to the slave.
11. The master sends a stop bit to the slave to stopping read.

Figure 8 shows the single byte read sequence, which read data 0x56 from register 0x2C.

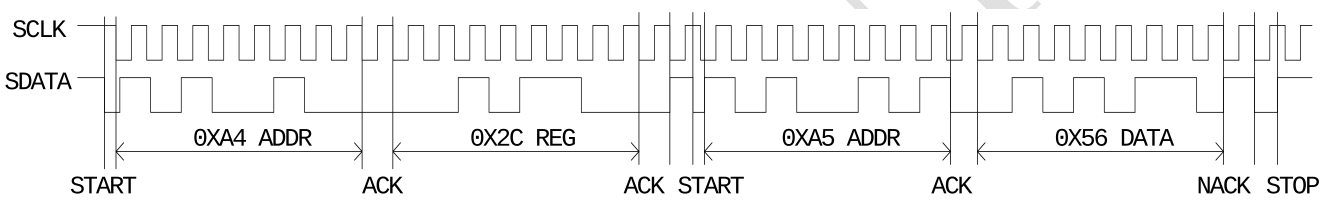

Figure 8 Single Byte Read Mode

4.1.2.4 Burst read mode

The burst read mode sequence is defined as the following.

1. The master sends a start bit to the slave.
2. The master sends the slave device address with write mode.
3. The slave sends an acknowledge bit to the master.
4. The master sends 8-bit register address.
5. The slave sends an acknowledge bit to the master.
6. The master sends a start bit to the slave.
7. The master sends the slave device address with read mode.
8. The slave sends an acknowledge bit to the master.
9. The slave sends 8-bit register's data.
10. The master sends an acknowledge bit to the slave.
11. The slave continues to send data by repeating step 9 and 10 until the master sends a no-acknowledge and the slave increases the register address by one automatically.
12. The master sends a stop bit to the master.

Figure 9 shows the burst read sequence, which read data 0x56 from register 0x2C and 0x75 from register 0x2D.

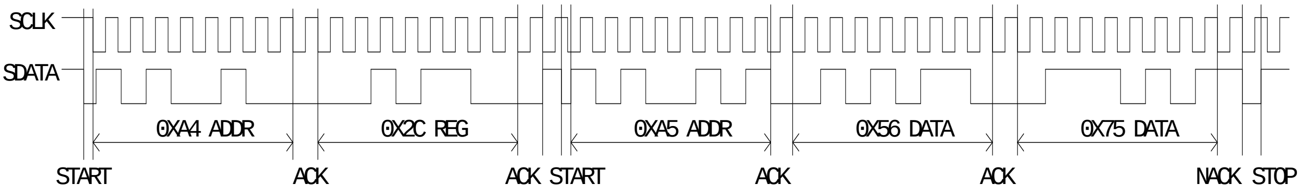

Figure9 Burst read

5 Timing Control

The Timing Control unit controls the operation of the imager. The Timing Control unit receives commands and settings from the Serial Control Interface. Based on the settings and commands, the Timing Control unit generates timing and control signals for exposure operation of CMOS image array.

6 ADC

ADC converts the analog image signal into the digital data so that the afterwards processing can be done in the digital domain. The ADC generates 10-bit data at a speed up to 50MHZ with 3.3v supply voltage.

7 PLL

The BG0316 has an internal PLL, which can generate PLL clock (fout) 35MHz~70MHz.

The PLL is controlled through its PLM, PLN and PLK parameters. The PLL output frequency (f_{out}) has the following relationship to the input frequency (f_{xclk}):

$f_{out} = f_{xclk}$*(PLM+2)/((PLN[5:0]+2)*PLLK)

Note: 1) PLM=0~127;
2) PLN=0~63;
3) PLK[1:0]=2'b00: PLLK=2
PLK[1:0]=2'b01: PLLK=4
PLK[1:0]=2'b10: PLLK=8
PLK[1:0]=2'b11: PLLK=16

The PLL takes time to power up. During this time, the behavior of its output clock is not Guaranteed. The PLL is in power-down by default and must be turned on manually.
When using the PLL, the correct power-up sequence after chip reset is as follows:
(1). Program PLL frequency settings (PLM, PLN, PLK)
(2). Power up PLL (PLLCTRL [1] =0)
(3). Wait for PLL settling time > 1ms

(4). Turn off PLL bypass (PLLCTRL [0] = 0)

8 Control Registers

The register of BG0316 has 8-bit address. Each 8 bit register occupies a single address. Each 16-bit register occupies two consecutive addresses. The lower address location is for the higher byte of the 16 bit register data while the higher address location is for the lower 8 bits of the 16 bit register data. For example, if you want to write 0x280 to HSIZE, you first write 0x02 to 0x06 and then 0x80 to 0x07.

8.1.1.1Registers Update (with I2C configuration timing)

Register value is updated at every flash posedge. e.g., the value written to one register at b point will take effect at c point.

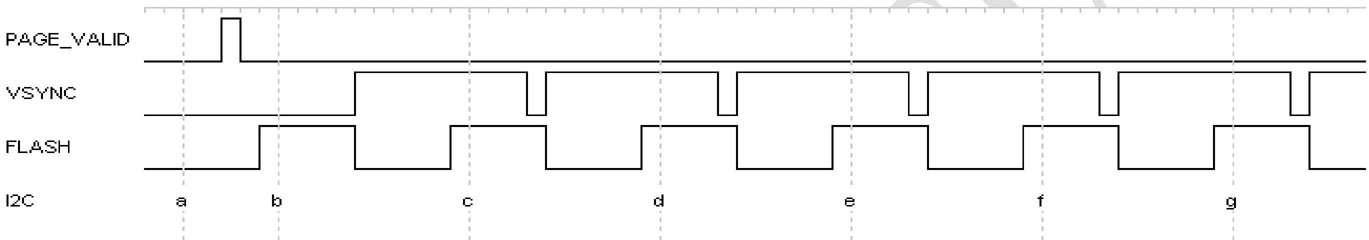

Figure 10 Timing relationship between IIC configuration and taking effect

9 Control Register Definitions.

Table 3 register definition table

Name	Width	Address(hex)	Description	Default
ID	[15:0]	8'h00	chip version ID	16'h0316
HSTART	[9:0]	8'h02	The first column to be read out, affected by READC[1]: 1). When READC[1] = 0, the read out circuit read from HSTART to HSTART+HSIZE-1; 2).When READC[1] = 1, the read out circuit read from HSTART+HSIZE-1 to HSTART.	10'h006
VSTART	[8:0]	8'h04	The first row to be read out, affected by READC[0]: 1). When READC[0] = 0, the read out circuit read from VSTART to VSTART+VSIZE-1; 2). When READC[0] = 1, the read out circuit read from VSTRT+VSIZE-1 to VSTART. In global shutter mode it must be 16x	9'h00c
HSIZE	[9:0]	8'h06	The window width size.	10'h280
VSIZE	[8:0]	8'h08	The window height size. In global shutter mode it must be 0x20	9'h1E0
MCLKC	[7:0]	8'h0a	The mclk control MCLKC[7]: pixclk inversion control. 1-inverted. fpixclk=fmclk. MCLKC[6:4]: pixclk delay control. 0-0ns, 1-1ns, 2-2ns. MCLKC[3]: bypass divide 2. If MCLKC[3]=1, fmclk = fmain_clock; If MCLKC[3]=0, fmclk= fmain_clock /2. MCLKC[2:0]: main_clock frequency control. fmain_clock = fout /(MCLKC[2:0]+1).	8'h88
TSMODE	[3:0]	8'h0b	Shutter control. TSMODE[3]: auto-change vstart control. 1-enable. TSMODE[2[: external trigger control. 1-enable TSMODE[1]: frame count sync control. 1-enable TSMODE[0]: Global(default: exposure by external trigger signal)/Rolling shutter control. 1-Global shutter mode, 0-Rolling shutter mode.	4'b0000
TEXP	[15:0]	8'h0c	The exposure time in rowtime unit	16'h0209
TROWADJ	[15:0]	8'h0e	The row time adjust, in mclk unit	16'h0000
NBLANKROW	[15:0]	8'h10	Global shutter mode: The interval between the end of last exposure and the start of next exposure Rolling shutter mode: The number of the blank row, in rowtime unit	16'h0118
TSH	[7:0]	8'h12	The sample time, in mclk unit	8'h19
TRST	[7:0]	8'h13	The reset time, in mclk unit	8'h1b
X2RST	[7:0]	8'h14	The gap between pos edge enx and pos edge enrb, in mclk unit	8'h00
RST2SHR	[7:0]	8'h15	The gap between negedge rst and posedge shr, in mclk unit	8'h00
SHR2TXB	[7:0]	8'h16	The gap between negedge shr and posedge txb, in mclk unit	8'h00
TXB2SHS	[7:0]	8'h17	The gap between negedge txb and posedge shs, in mclk unit	8'h00
TTXA	[7:0]	8'h18	The txa time, in mclk unit	8'h1a
TTXB	[7:0]	8'h19	The txb time in rolling shutter mode; Enra time=TTXB*2 in global shutter mode. In mclk unit	8'h1a

VSTART_INC	[6:0]	8'h1a	VSTART_INC[6]: increase/decrease control. 1-decrease, 0-increase. VSTART_INC[5:0]: the num row of auto change vstart. Valid for both global and rolling shutter mode. When set, the row start value will be changed by 16 automatically	7'h10
FRAME_COUNT	[5:0]	8'h1b	The number of frames in a page. Valid for both global and rolling shutter mode	6'h1e
SOFTRESET	[0]	8'h1c	The software reset. Writing a 1 resets all internal registers to its default values and take effect immediately. This bit is self cleared to zero.	1'b0
RESTART	[2:0]	8'h1d	RESTART [0]: write "1" to this bit will start a new session immediately; RESTART [1]: write "1" to this bit will update all frame registers at next frame; RESTART [2]: Reserved.	3'b000
READC	[9:0]	8'h20	Read control for different modes. READC[0]: row flip control READC[1]: column mirror control READC[3:2]: bad frame control READC[4]: enable/disable 2x row skip, 1-enable. READC[5]: enable/disable 2x col skip, 1-enable READC[7:6]: reserved READC[8]: reserved. READC[9]: enable/disable skipping dark row, 1-skipping read dark row.	10'h000
GAINF	[1:0]	8'h27	Frame gain. Frame gain = (gainf[0]+1) * (gainf[1]+1)	2'b00
FGG1	[8:0]	8'h28	Green1 gain. Gain = (fgg1[8]+1) * (fgg1[7]+1) * fgg1[6:0]/64, where fgg1[6:0] can't be set to "0"	9'h40
FGG2	[8:0]	8'h2a	Green2 gain. Gain= (fgg2[8]+1)*(fgg2[7]+1)*fgg2[6:0]/64, where fgg2[6:0] can't be set to "0"	9'h40
FGR	[8:0]	8'h38	Red gain. Gain = (fgr[8]+1)*(fgr[7]+1)*fgr[6:0]/64, where fgr[6:0] can't be set to "0"	9'h3b
FGB	[8:0]	8'h3a	Blue gain. Gain= (fgb[8]+1)*(fgb[7]+1)*fgb[6:0]/64, where fgb[6:0] can't be set to "0"	9'h60
RBG	[5:0]	8'h2c	RBG[5]: pdbgp, when"1"shutdown internal bandgap RBG[4]: exvbg RBG[3:0]: rbg	6'h08
ICPIX	[3:0]	8'h2d	The itune current of pixel array	4'h4
ICYDEC	[3:0]	8'h2e	The itune current of y-decoder	4'ha
ICADC	[3:0]	8'h2f	The itune current of adc	4'ha
EXDIS	[4:0]	8'h30	EXDIS[4:3]: envnws EXDIS[2]: exref EXDIS[1]: vtdis EXDIS[0]: reserved	5'h00
VTHC	[3:0]	8'h33	The voltage of tx for high control	4'h4
RTSEL	[3:0]	8'h34	RTSEL[3]: selvrp RTSEL[2]: selvrn RTSEL[1]: vrsel RTSEL[0]: vtsel	4'hd
DCTRL	[1:0]	8'h37	Pad function control. DCTRL[0]: select page_valid or dout[1] control. 0: select input page_valid 1: select output dout[1] DCTRL[1]: select PWDN or dout[0] control. 0: select input PWDN 1: select output dout[0]	2'b00

PADCTRL	[3:0]	8'h3d	Pad state control. PADCTRL[0]: Tri-state option for dout when standby 0: Tri-state 1: No-Tri-state PADCTRL [1]: Tri-state option for pixclk, vsync, hsync, flash when standby 0: Tri-state 1: No-Tri-state PADCTRL[2]: hsync active pole control. 1-active high; 0-active low. PADCTRL[3]: vsync active pole control. 1-active high; 0-active low.	4'hc
RST2TX	[7:0]	8'h3f	The gap between posedge enra and posedge enta	8'h01
DGG1	[1:0]	8'h40	Green1 digital gain. Green1 digital gain = (dgg1[0]+1) * (dgg1[1]+1)	2'b00
DGG2	[1:0]	8'h41	Green2 digital gain. Green2 digital gain = (dgg2[0]+1) * (dgg2[1]+1)	2'b00
DGR	[1:0]	8'h42	Red digital gain. Red digital gain = (dgr[0]+1) * (dgr[1]+1)	2'b00
DGB	[1:0]	8'h43	Blue digital gain. Blue digital gain = (dgb[0]+1) * (dgb[1]+1)	2'b00
BLCC	[3:0]	8'h44	Black-level compensation control. BLCC[0] is automatic black level compensation control, when"1", it bypass black level auto-compensation, when "0", it does the the auto-compensation, BLCC[1] is total compensation control, when "1", the data bypass all compensation, when "0", it does the compensation. BLCC[2] is the output data from ADC control, when "1", the output data = the high 10 bits data from ADC output BLCC[3]: hot pixel in dark row disable/enable.1:disable,0:enable	4'b1000
BCG1	[9:0]	8'h45	Green1 offset. 2's complement representation of offset for green1	10'h000
BCG2	[9:0]	8'h47	Green2 offset.2's complement representation of offset for green2	10'h000
BCR	[9:0]	8'h49	Red offset.2's complement representation of offset for red	10'h000
BCB	[9:0]	8'h4b	Blue offset.2's complement representation of offset for blue	10'h000
DOFFSET	[9:0]	8'h4d	The digital offset for all color channels	10'h000
RAWCTRL	[1:0]	8'h80	Raw data output control. When RAWCTRL[1:0] =2'b11, enable 10bit raw data output. When RAWCTRL[1:0] =2'b10, enable 8bit raw data output.	2'b10
PLM	[6:0]	8'h90	PLL multiply	7'h26
PLN	[6:0]	8'h91	PLN[6]: bypass pll divider PLN[5:0]: PLL divider	7'h40
PLK	[3:0]	8'h92	PLK[1:0]: select divided by2,4,8,16 PLK[3:2]: select pump clock fxclk, divided by 2, 4, 8.	
PLLRC	[7:0]	8'h93	PLL RC control. PLLRC[7]: PLLRC PLLRC[6:5]: PLLR PLLRC[4:0]: PLCC	8'h00
PLLCTRL	[2:0]	8'h94	PLL control PLLCTRL[2]: lock signal select. PLLCTRL[1]: power down PLL control. 1-power down PLLCTRL[0]: bypass PLL control. 1-bypass PLL	3'b011
PLLOCKTIME	[7:0]	8'h95	PLL lock time, in 256 fxclk unit	8'h10
POWERC	[2:0]	8'h9e	power down control. POWERC [0]: Reserved. POWERC [1]: soft sleep. Write "1" to this bit, the sensor will be put into sleep. Write "0" to this bit, the sensor will be recover. POWERC [2]: Reserved.	3'b000

10 Frame/Row Synchronization and Timing

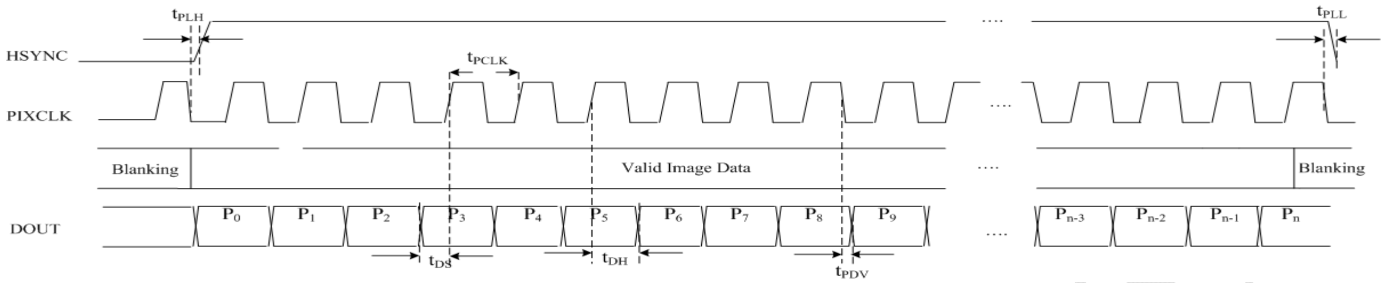

Figure 11 Typical pixel data output

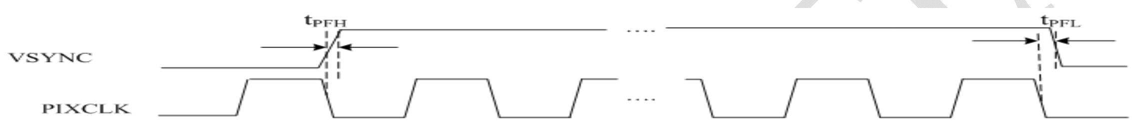

Figure 12 PIXCLK and vsync

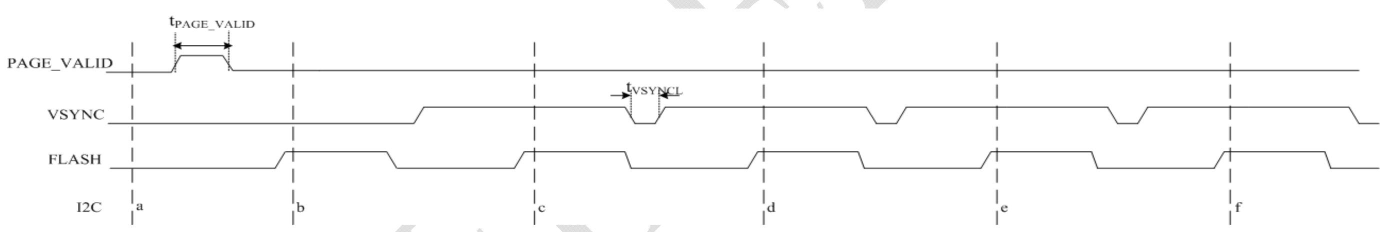

Figure13 Vsync and flash, page_valid

Table 4: AC Electrical Characteristics (See Figure 11, Figure 12, Figure13)

Symbol	Definition	Condition	Min	Typ	Max	Unit	Notes
fXCLK	Input Clock Frequency	PLL off		40		MHz	
tXCLK-DC	Clock Duty Cycle		45	50	55	%	
tPIXCLK	PIXCLK period			25		ns	
tDS	DOUT Setup Time	tPIXCLK=25ns		10		ns	
tDH	DOUT Hold Time	tPIXCLK=25ns		10		ns	
tPLH	PIXCLK to HSYNC High	tPIXCLK=25ns		10		ns	
tPLL	PIXCLK to HSYNC Low	tPIXCLK=25ns		10		ns	
tPFH	PIXCLK to VSYNC High	tPIXCLK=25ns		10		ns	

tPFL	PIXCLK to VSYNC Low	tPIXCLK= 25ns		10		ns	
tPDV	PIXCLK to Data valid			2		ns	
tPAGE_VALID	PAGE_VALID high time		4			tPIXCLK	
tVSYNCL	The minimal interval VSYNC low between two frame			2		tPIXCLK	

Table 5 Frame Timing Formulas

Parameter	Description	Equation(the frequency of xclk
A	Active time	HSIZE x (MCLKC[2:0]+1) x tpixclk
Q	Horizontal blanking time	TSMODE[0]=1: (TSH*2+X2RST+SHR2TXB+RST2SHR+22+TROWADJ) x (MCLKC[2:0]+1) x tpixclk TSMODE[0]=0: (TSH *2+X2RST+SHR2TXB+RST2SHR+TRST+TTXB+RST2TX+TROWADJ) x (MCLKC[2:0]+1) x tpixclk
Texp	Exposure time	TEXP x (A+Q)
Tfrm	Frame time	TSMODE[0]=1: (TEXP+NBLANKROW) x (A+Q) TSMODE[0]=0: (VSIZE + NBLANKROW) x (A + Q)

11 Data Output Mirroring

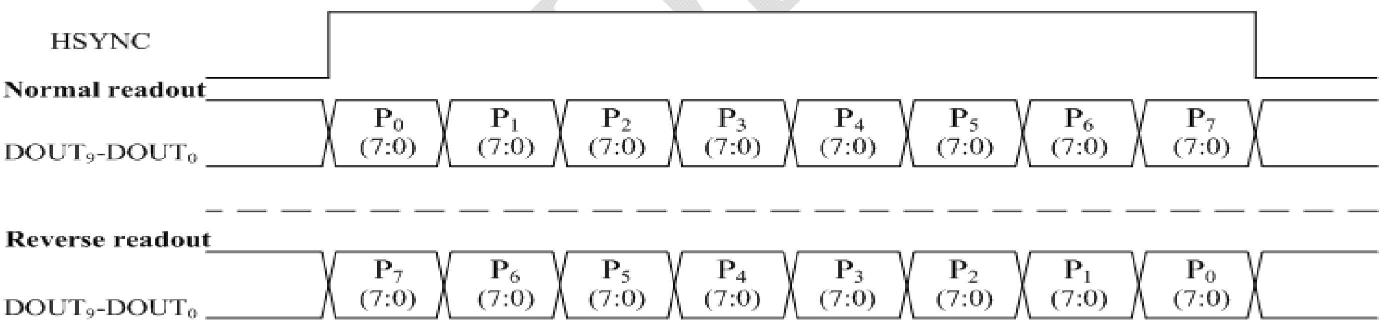

Figure14 Readout of 8 pixels in normal and Column mirror output mode

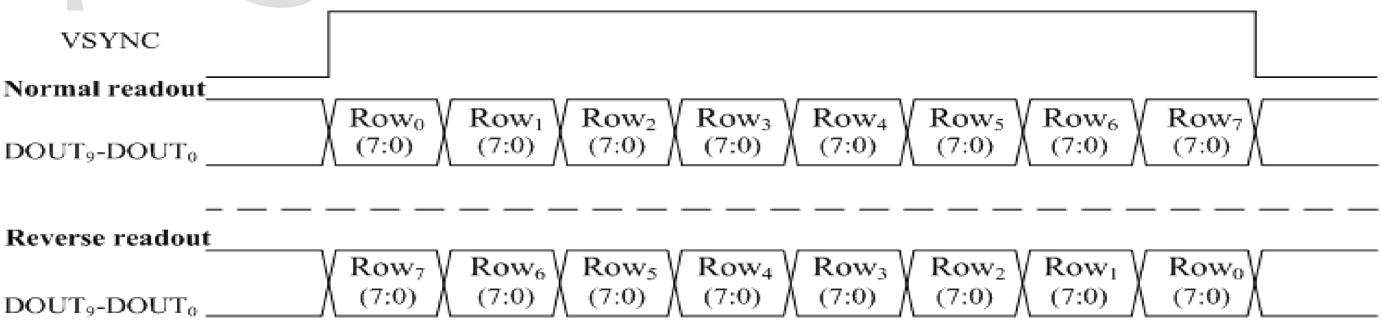

Figure15Readout of 8 rows in normal and Row mirror readout mode

12 Output data ordering

Table 6 Output data order

Mode	D7	D6	D5	D4	D3	D2	D1	D0	PAGE_VALID	PWDN
10-bit parallel output RAWCTRL=2'b10 DCTRL=2'b11	DOUT[9]	DOUT[8]	DOUT[7]	DOUT[6]	DOUT[5]	DOUT[4]	DOUT[3]	DOUT[2]	DOUT[1]	DOUT[0]

Mode	D7	D6	D5	D4	D3	D2	D1	D0	PAGE_VALID	PWDN
8-bit parallel output RAWCTRL=2'b10 DCTRL=2'b00	DOUT[9]	DOUT[8]	DOUT[7]	DOUT[6]	DOUT[5]	DOUT[4]	DOUT[3]	DOUT[2]	PAGE_VALID	PWDN

13 Electrical Characteristics

Table 7 DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit	Notes
VDD-A	VDDA voltage		2.7	2.8	3.3	V	
VDD-IO	VDDO voltage		2.7	2.8	3.3	V	
VIH	Input Voltage High		0.7 *VDD-IO			V	
VIL	Input Voltage Low				0.3*VDD-IO	V	
IIN	Input Leakage Current	No pull-up resistor, VIN=VDD-IO or DGND	-1		1	µA	
VOH	Output High Voltage		0.9*VDD-IO			V	
VOL	Output Low Voltage				0.1*VDD-IO	V	
IOH	Output Current High	VOH=2.4V		15		mA	
IOL	Output Current Low	VOL=0.4V		9		mA	
IDD-A	Analog Operating Current					mA	
IDD-D	Digital Operating Current					mA	
IDD-IO	IO Operating Current					mA	
ISTD	Standby Supply Current	PWDN = VDD-IO				µA	